U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Application No.
	MST-1898-22D	10/800,382
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicants	
(Use several sheets if necessary)	Leung et al.	
	Filing Date	Group
	3/11/2004	Unknown

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AE 9-10-09

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
JT	AA	3,585,378	15 ~~May~~ 1971	Bouricius et al.			
	AB	3,651,473	21 Mar 1972	Faber			
	AC	3,761,879	25 Sep 1973	Brandsma et al.			
	AD	3,803,562	9 Apr 1974	Hunter			
	AE	3,810,301	14 May 1974	Cook			
	AF	3,835,530	17 Sep 1974	Kilby			
	AG	3,849,872	26 Nov 1974	Hubacher			
	AH	3,859,640	7 Jan 1975	Eberlein et al.			
	AI	3,983,537	28 Sep 1976	Parsons et al.			
	AJ	4,007,452	8 Feb 1977	Hoff, Jr.			
JT	AK	4,038,648	26 Jul 1977	Chesley			

Foreign Patent Documents

							Translation	
JT		Document	Date	Country	Class	Subclass	Yes	No
	AL	1002664	28 Dec 1976	Canada				
	AM	0162932 A3	4 Dec 1985	EP				
	AN	0178949 A3	23 Apr 1996	EP				
	AO	0258062 A2	2 Mar 1988	EP				
JT	AP	0258062 A3	2 Mar 1988	EP				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

JT	AQ	"32K x9 Bit BurstRAM Synchronous Static RAM with burst Counter and Self-Timed Write," Motorola Memory Data (MCM62486A)(No Date), pp. 7-100 to 7-109.
JT	AR	Antola et al., "Reconfiguration of Binary Trees: The Flow-Driven Approach," 1991 International Conference on Wafer Scale Integration, 1991, pp. 141-147.
JT	AS	Aubusson, Russell C. and Ivor Catt, "Wafer-Scale Integration—A Fault-Tolerant Procedure," IEEE Journal of Solid State Circuits, Vol. SC-13, No. 3, Jun 1978, pp. 339-344.

Examiner /Joseph Torres/	Date Considered 10/25/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.